16. (CURRENTLY AMENDED) A parallel processor performing parallel processing of at least one ~~or more~~ basic ~~instructions~~ instruction contained in each of a plurality of instruction words, each of the instruction words consisting of the at least one basic instruction to be executed by at least one instruction execution unit and ~~delimited by instruction~~ delimiting information only delimiting the at least one basic instruction, said parallel processor comprising:

~~a plurality of~~ instruction execution units performing processes in accordance with corresponding, supplied basic instructions in parallel;

an instruction fetch unit fetching the instruction words one by one in accordance with the instruction delimiting information; and

an interface ~~having~~ setting effective bits each corresponding to one of the instruction execution units and indicating ~~the~~ a corresponding instruction execution unit for each basic instruction to be executed from each instruction word ~~which have no attached dispersal information~~, checking codes of the at least one basic ~~instructions~~ instruction to identify the at least one basic ~~instructions,~~ instruction and ~~associating the basic instructions with respective ones of said~~ to determine the corresponding instruction execution unit ~~units, said instruction execution units being associated with respective effective bits indicative of whether the~~ for each basic ~~instructions are supplied to said~~ instruction ~~execution units~~.

REMARKS

On pages 2-8 of the May 15, 2006 Office Action, claims 1-8, 11-13, 15 and 16 were rejected under 35 USC § 102 as anticipated by U.S. Patent 5,930,508 to Faraboschi. The rejections are traversed below.

Although the Response to Arguments on item 16 on page 8 of the Office Action indicated that there were "newly applied ground of rejection ..." the only difference that has been found in the May 15, 2006 Office Action compared to the September 22, 2005 Office Action is sub-item d at page 3, lines 3-10; "further comprising a conversion unit," on the second line of item 12 on page 6 of the Office Action and changes in the wording of sub-item c on page 8 of the Office Action. These changes apparently have not affected the essential reason that the claims continue to be rejected. The "dispersal bit sets D1, D3, D5 and D6 which are illustrated in Figs. 4 and 5 and described at column 4, line 57 to column 5, line 35 as being stored in a "compacted instruction" 400 (Fig. 4) apparently are still considered to be equivalent to the "effective bits" of the present invention, despite the recitation of "no dispersal information" in the claims as previously presented.

In yet another effort to recite the invention in a manner that will make the distinction between the invention and Faraboschi et al. clear to the Examiner, the independent claims have been amended to recite that the instruction words contain no dispersal information of the type included in the compacted instruction of the system taught by Faraboschi et al. Specifically, claim 1 recites "wherein each of the instruction word **consists** of the one or more basic instructions to be executed by one or more instruction execution units and delimiting information delimiting the one or more basic instructions" (claim 1, lines 2-5, emphasis added) and claim 16 recites "each of the instruction words **consisting** of the at least one basic instruction to be executed by at least one instruction execution unit and delimiting information only delimiting the at least one basic instruction" (claim 16, lines 3-5, emphasis added). As indicated by the emphasized word **consisting**, instruction words according to the invention **only** contain basic instruction(s) and delimiting information. As described in the specification and emphasized by the word "only" in claim 16, the delimiting information is not used for determining dispersal of the basic instructions among the instruction execution units. Rather, the "instruction issue unit issues N instruction pairs ... supplied to N respective instruction execution units" (claim 1, lines 11-15) where each instruction pair "includes a basic instruction and a single effective bit controlling whether the basic instruction is to be executed by the corresponding instruction execution unit" (claim 1, lines 18-19).

Claim 16 recites "an interface setting effective bits each corresponding one of the instruction execution units and indicating a corresponding instruction execution unit for each basic instruction to be executed from each instruction word" (claim 16, lines 10-12). In addition, claim 16 recites "checking codes of the at least one basic instruction to identify the at least one basic instruction and to determine the corresponding instruction execution unit for each basic instruction" (claim 16, last five lines).

On the other hand, Faraboschi et al. teaches selecting an execution unit for execution of an instruction by use of the dispersal bit set stored with each syllable (S1, S3, S5 or S6 in Fig. 4) of compacted instruction 400. The dispersal bit set indicates the functional unit by which the syllable is to be executed and there is no "checking codes of the at least one basic instruction" as recited in claim 16. Instead, the dispersal block shown in Fig. 6 of Faraboschi et al. transforms the compacted instruction into dispersed instructions based on the dispersal bit sets, not by analysis of the instruction code, i.e., the "syllable" S1, for example. As a result, the compacted instruction has to change when the structure of the parallel processor changes. One of the benefits of the present invention is that no recompilation of instructions is required, since the "interface" recited in claim 16 "determine[s] the corresponding instruction unit for each basic

instruction" (claim 16, last three lines) by "checking codes of the at least one basic instruction" (claim 16, line 13). Due to the use of dispersal codes stored in compacted instructions, a system based on Faraboschi et al. would have to recompile the instructions when the instruction execution units change enough to require different dispersal bit sets.

For the above reasons, it is submitted that claims 1 and 16, as well as claims 2-8, 11-13 and 15 which depend from claim 1, patentably distinguish over Faraboschi et al. If it is believed that the amended claims are still anticipated by Faraboschi et al., **the Examiner is respectfully requested to contact the undersigned by telephone prior to issuing the next Office Action**, to arrange an Examiner Interview for the purpose of discussing what further amendments could be made to clarify the distinction discussed above.

Summary

It is submitted that Faraboschi et al. does not teach or suggest the features of the present claimed invention. Thus, it is submitted that claims 1-8, 11-13, 15 and 16 are in a condition suitable for allowance. Reconsideration of the claims and an early Notice of Allowance are earnestly solicited.

Finally, if there are any formal matters remaining after this response, the Examiner is requested to telephone the undersigned to attend to these matters.

If there are any additional fees associated with filing of this Amendment, please charge the same to our Deposit Account No. 19-3935.

Respectfully submitted,

STAAS & HALSEY LLP

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, PO. Box 1450, Alexandria, VA 22313-1450
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By
Date Sept 15, 2006